REMARKS

As a preliminary matter, claims 16-17, 21, and 24-26 stand objected to for informalities and/or defects. Applicants traverse the objections in their entirety. The Examiner has not established that any informalities or defects actually exist in the claims.

For example, with respect to claim 16, the Examiner objects to the use of the word "substantially," but leaves out the context of the claim limitation in which the term appears. Claim 16 actually recites that the first insulation film is formed on the channel region and the low density impurity regions, and that it covers substantially all of the surface of the channel and low density impurity regions. Applicants have repeatedly directed the Examiner's attention to Figs. 10C and 10D of the present Application, and the accompanying description on pages 44-45, that clearly support these claimed features. Any person of ordinary skill in the art could read the claim term "substantially all," look at these portions of the Specification, and easily understand the meaning of the term. Claim limitations using the phrase "substantially all" are commonly used in patent practice to generally mean "all," but also allowing for manufacturing tolerances that are not perfect. Applicants again request that the Examiner consider the portions of the Specification noted above, and withdraw this objection to claim 16.

Further with respect to claim 16, the Examiner objects to the phrase "of the channel," but again removes the context in which the claimed phrase appears. Taken in the entire context of the sentence, the Examiner could see that there is no defect in the claim. The portion of the claimed phrase refers to "all of the surface of the channel and

low density impurity regions." The word "regions" already appears in the claimed phrase, but in the plural form, and refers to both the channel region and the low density impurity regions. It is entirely grammatically correct to refer to a "first region and a second region" as "first and second regions." The meaning of the two phrasing styles is identical. This particular rejection with respect to claim 16 should also be withdrawn.

With respect to claims 21 and 24, Applicants note that the Examiner does not comment on any of the discussion from Amendment E relating to these claims. Accordingly, all of the arguments presented in Amendment E are incorporated by reference herein. As previously argued, the Examiner incorrectly interprets the device recited in claims 21 and 24 as a method claim for forming the device. Nothing in the claim language of either claim 21 or 24 (or base claim 16) supports such an unreasonable interpretation. All of these device claims recite structural limitations to the thin film transistor device. It is entirely improper for the Examiner to attempt to add additional limitations to these claims relating to a method for forming the transistor device.

Applicants have also repeatedly pointed out to the Examiner (without any answer or rebuttal) how the reflection of laser light recited in claim 21 is not recited as a portion of the formation of the device. Claim 21 actually recites only the thickness of the second insulation film, which is entirely a structural limitation, and its material properties of reflectivity for at least two different regions of the transistor device. The relationship between the structural thickness and the laser light is clearly defined in claim 21, contrary to the Examiner's assertion.

Claim 21 further recites that the thickness of the second insulation film is such that the degree of reflection of the laser light is substantially equal at both the low density impurity regions, and at the source and drain regions of the transistor device. Applicants respectfully request that the Examiner consider only the actual claim language recited, and not add the proposed additional limitations. The effect of the laser light on the structure is not recited. Only the reflectivity of the laser light is featured in the claim, but then as a material property of the film thickness.

The Examiner's failure to consider the actual claim language is further apparent with respect to claim 24, which depends from claim 21. Claim 24 recites that the wavelength of the laser light is a factor to determine the thickness of a second insulation film, as opposed to a laser that forms a film. One skilled in the art would understand from claim 24 to set the thickness of the second insulation film to be able to reflect laser light of a particular wavelength equally at the several regions of the device recited in claim 21. The wavelength of laser light is a measurable dimension, and not a process limitation, and the thickness of the second insulation film is only a structural limitation. The objection to claims 21 and 24 should also be withdrawn.

Claims 16-17 and 25-26 again stand rejected under 35 U.S.C. 102(b) as being anticipated by Takemura et al. (U.S. 5,719,065). Applicants again respectfully traverse this rejection for at least the reasons of record (Amendment E incorporated by reference herein, discussed above), and as follows. Takemura simply does not teach (or suggest) a second insulation film that covers substantially all of the surface of the first

insulation film on the low density impurity regions, as in claim 16 of the present invention, as last amended.

For the purposes of this discussion only, if the Examiner were actually correct (which Applicants do not concede) to assert that the y and y' regions in Fig. 5A in Takemura correspond to the low density impurity regions, and that the layer 104 formed immediately under the gate electrode 105 corresponds to the first insulation film of claim 16 of the present invention, Takemura still cannot read upon claim 16. Only TFT2 in the drawing shows the film 104 to cover substantially all of the surface of the channel and low density regions. Therefore, the Examiner's assertions regarding Takemura's "second insulation film" (barrier layer 108 between the gate electrode 105 and the film 114) become entirely erroneous in this drawing.

The Examiner asserts that Takemura's barrier layer 108 "covers substantially all of the surface of the first insulating film [104] on the low density impurity regions." Fig. 5A of Takemura, however, entirely fails to support this assertion. The Examiner has identified the y-region of Fig. 5A as the low density region, and it is clear that, at most, only about half of the surface of the film 104 on y-region is covered by the barrier layer 108. A large portion of the film 104 on the y-region for TFT2 is clearly exposed away from the barrier layer 108. The Examiner's assertion to the contrary is simply erroneous.

The Examiner's additional remarks therefore, asserting that Takemura's "second insulating film also covers the substantially large portion of the surface of the

first insulating film that is directly under the gate electrode therein," indicate a significant problem underlying the rejection. The feature of claim 16 at issue recites that the insulation film covers "substantially all of the surface of the first insulation film on the low density impurity regions." There is no limitation in the claim that refers to a "substantially large portion of the surface of the first insulating film that is directly under the gate electrode," as asserted by the Examiner. The Examiner again appears to be adding his own limitations to claim 16.

As explained in the previous Responses, Figs. 10C and 10D of the present Specification illustrate how the portion of the first insulation film covering the low density impurity regions is also covered by the second insulation film. Claim 16 does not recite any limitations regarding any portion of the first insulating film that may also cover the channel region. Such a limitation has never been presented to the Examiner for consideration, and no such limitation is required by the present Specification. By improperly adding this limitation to the claims, the Examiner changes the meaning of the claim from what is actually recited.

The channel region is shown, in the drawings of the present Application, to be significantly larger than the respective low density impurity regions. "Substantially all" of the surface of the first film *on both the channel and low density regions* would thus have a very different meaning than "substantially all" of the surface on only the low density regions. Claim 16 recites that the second insulation film covers substantially all of the surface of the first insulation film on the low density regions, and this limitation is

clearly supported by Fig. 10 of the present Application. As explained above, Fig 5A of Takemura cannot read upon these limitations without the inappropriate addition of further claim limitations that are not recited (such as those regarding the channel region). Accordingly, for all of the foregoing reasons, the rejection of claim 16 (and its dependent claims) based on Takemura should be withdrawn.

The rejection of claim 16 should further be withdrawn in light of the fact that Takemura specifically teaches away from the Examiner's interpretation, and therefore from the present invention. Takemura's description of its manufacturing processes (column 4, line 57 through column 8, line 23 and Column 8, line 25 through column 9, line 16) expressly contradicts the Examiner's analogies to the present invention. Fig 4A of Takemura, for example, illustrates that the gate insulating film 104' covers substantially all of the surface of the regions 121, 122, which regions the Examiner considers to be analogous to the low density impurity regions of the present invention. (See column 8, lines 34-50). The gate insulating film 104' is then further patterned into the gate insulating film 104'' in a self aligning manner with respect to the barrier and anodicoxide layer 108. (See column 8, lines 51-54, Fig 4B).

These portions of the reference clearly illustrate that the gate insulating film 104'' (which the Examiner deems to be analogous to the first insulation film of the present invention) does not cover substantially all of the surface of the regions 121, 122 for the TFTS 1 and 3. Figs 4A and 4B of Takemura demonstrate how the preliminary gate insulating film 104' covers substantially all of the surface of the regions 121, 122,

but that this preliminary film is further patterned into the reduced gate insulating film 104''. This reduced layer would not, by definition, cover all of the area covered by the larger preliminary film 104'. Accordingly, for at least these additional reasons, the rejection should be withdrawn.

Additionally, Takemura further teaches away from the Examiner's assertions with regard to the disclosed method for manufacturing the TFT 2. Figs 3A-3H and 5A also show that the barrier type and anodic oxide film 108 does not cover substantially all of the surface of the gate insulting film on the regions 111, 112. Takemura describes that the film 108 is formed inside the porous anodic oxide film 107 (column 6, line 20-21, Fig 3C), and that the film 104 is patterned into the gate insulating film 104' using the porous film 107 as a mask. (Column 6, lines 29-31, Fig 3D). Accordingly only the films 107 and 108 taken together can be said to cover substantially all of the surface of the gate insulating film 104', but not the film 108 by itself.

Fig 3D of Takemura further shows that the film 107 is formed on both sides of the gate insulating film 104', but that the film 108 is not formed on both sides of the gate insulating film. Fig 3F illustrates that the regions 111, 112 are also formed on both sides of the film 104' (see column 7, lines 3-26). Accordingly, contrary to the Examiner's assertions, the film 108 cannot cover substantially all of the surface of the gate insulating film 104' and the regions 111, 112, and therefore Takemura does not support the Examiner's assertions that the "second insulation film" 108 covers substantially all of the surface of the "first insulation film" 104' on the "low density

impurity regions" 111, 112. In these illustrations, Takemura shows that the film 108 is not formed on both sides of the gate insulating film 104', but the regions 111, 112 are actually formed on both sides. Accordingly, for at least these still further reasons, the rejection of claims 16 and its dependent claims should once again be withdrawn.

Claims 21 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura. Applicants respectfully traverse this rejection for at least the reasons discussed above, and as follows. Claims 21 and 24 both depend directly or indirectly from independent claim 16, and therefore should be patentable for at least the same reasons that the base claim is patentable. Claims 21 and 24 are also patentable because the Examiner has not established a *prima facie* case of obviousness.

Applicants are at a loss to understand the Examiner's discussion of "absolute thickness." Neither claim 21 nor 24 recites anything about an "absolute thickness." In fact, claims 21 and 24 both recite structural limitations for the thickness of the second insulation film that enables this film to reflect laser light equally at the low density impurity regions, and at the source and drain regions of the thin film transistor. Nothing in any cited portion from Takemura teaches or suggests that the degrees of reflection of laser light by the barrier layer 108 are substantially equal at these various regions of the transistor. Without any such teaching or suggestion within the reference, the Examiner cannot establish or maintain a *prima facie* case of obviousness according to Section 2143.03 of the MPEP.

The Examiner appears to have simply dismissed almost all of the limitations of claims 21 and 24 as being merely "process limitations." As discussed above and previously, this dismissal is inappropriate, and based upon erroneous determinations. The thickness of the second insulation film, and its reflectivity properties, are not "process limitations." The mere fact that a laser may or may not also be used in the manufacture of the transistor devices is irrelevant to what is actually claimed in claims 21 and 24. The thickness of the second insulation film, and its other material properties, are structural limitation to which the Examiner is required to give full consideration. Because the Examiner has not given full consideration to claims 21 and 24, the rejection must be withdrawn.

For all of the foregoing reasons, Applicants submit that this Application, including claims 16-17, 21, and 24-26, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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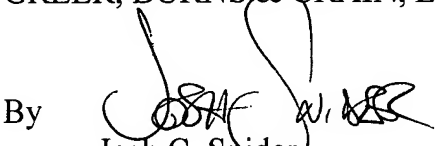
By 
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